## Claims

What is claimed is:

1. A substrate having an active side and a back side, comprising:

an active side interconnect disposed on the active side;

a backside interconnect disposed on the backside, coupled to and in substantial vertical alignment with the active side interconnect; and

a redistributed interconnect of the backside interconnect disposed on the backside, coupled to and offset from the backside interconnect.

2. The substrate of claim 1, further comprising:

a metal layer having a first side and a second side;

a first dielectric layer adjacent to the first side of the metal layer;

a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;

a second dielectric layer adjacent to the second side of the metal layer; and

a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

3. The substrate of Claim 1, wherein the redistributed interconnect comprises:

a conductive trace coupled to and extending from the backside interconnect to a selected location;

a third dielectric layer overlaying the conductive trace; and

an aperture in the third dielectric layer substantially at or near the selected location.

4. The substrate of Claim 3, wherein the selected location for the redistributed interconnect corresponds to an interconnect on a second substrate.

5. The substrate of Claim 1, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.

6. A semiconductor device, comprising:

a carrier substrate having a bond pad;

a first substrate, the first substrate comprising

an active side and a back side;

an active side interconnect, the active side interconnect disposed on the active side, coupled to the bond pad of the carrier substrate;

a backside interconnect disposed on the back side, coupled to and in substantial vertical alignment with the active side interconnect;

a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect; and

a second substrate electrically coupled to the redistributed interconnect of the first substrate.

7. The semiconductor device of claim 6, wherein the first substrate comprises:

a metal layer having a first side and a second side;

a first dielectric layer adjacent to the first side of the metal layer;

a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;

a second dielectric layer adjacent to the second side of the metal layer; and

a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

8. The semiconductor device of Claim 6, wherein the redistributed interconnect comprises:

a conductive trace coupled to and extending from the backside interconnect to a selected location;

a third dielectric layer overlaying the conductive trace; and

an aperture in the third dielectric layer at the selected location.

9. The semiconductor device of Claim 8, wherein the selected location for the redistributed interconnect corresponds to an interconnect on the second substrate.

10. The semiconductor device of Claim 6, wherein the first substrate and the second substrates are microelectronic dies.

11. The semiconductor device of claim 6, wherein the second substrate is coupled to the redistributed interconnect by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.

12. The semiconductor device of Claim 6, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.

13. A method comprising:

providing an active side interconnect to an active side of a substrate;

providing a backside interconnect to a back side of the substrate with the backside interconnect being coupled to and in substantial vertical alignment with the active side interconnect; and

providing a redistributed interconnect of the backside interconnect on the backside, the redistributed interconnect being coupled to and offset from the backside interconnect.

14. The method of Claim 13, wherein providing the redistributed interconnect comprises:

depositing a conductive trace on the back side;

coupling the conductive trace to the backside interconnect;

extending the conductive trace to a selected location;

placing a third dielectric layer over the conductive trace; and

forming an aperture in the third dielectric layer at the selected location.

15. The method of Claim 13, wherein providing the backside interconnect comprises forming a via that extends from the backside interconnect through a second dielectric layer to a metal layer and filling the via with an electrically conductive material.

16. The method of claim 13, further comprising;

providing a carrier substrate having a bond pad

providing a second substrate having an interconnect;

coupling the active side interconnect to the carrier substrate bond pad; and

coupling the interconnect of the second substrate to the redistributed interconnect.

17. The method of Claim 16, wherein coupling the interconnect of the second substrate to the redistributed interconnect is performed by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.

18. A method for redistributing interconnects, comprising:

providing a substrate having an active side and a backside, the active side having an active side interconnect;

forming a via in the backside extending from a surface of the backside to a metal layer within the substrate;

filling the via with an electrically conductive material such that a backside interconnect is formed at or substantially near the surface of the backside and in electrical communication with the metal layer;

depositing a conductive trace on the backside surface such that the conductive trace extends from the backside interconnect to a selected location on the back side surface;

depositing a dielectric layer on the back side surface such that it overlays the conductive trace; and

defining a redistributed interconnect of the backside interconnect at the selected location.

19. The method of Claim 18, wherein defining the redistributed interconnect comprises forming an aperture in the dielectric layer at the selected location to expose a portion of the conductive trace.

20. The method of Claim 19, wherein forming the aperture comprises etching a portion of the dielectric layer at the selected location to expose a portion of the conductive trace.

21. The method of Claim 18, further comprising choosing the selected location to correspond to a location of a complementary interconnect of a substrate in facing relationship there with.

22. The method of Claim 18, wherein depositing the conductive trace comprises forming a patterned electrically conductive layer on the backside surface using a photolithography process.

23. The method of Claim 18, further comprising depositing a conductive interconnect material into the dielectric aperture such that the conductive interconnect material is coupled to the redistributed interconnect and extends above the dielectric layer.

24. The method of claim 18, further comprising;

providing a carrier substrate having a bond pad;

providing a second substrate having an interconnect;

coupling the active side interconnect to the carrier substrate bond pad; and

coupling the interconnect of the second substrate to the redistributed interconnect.

25. The method of Claim 24, wherein coupling the interconnect of the second substrate to the redistributed interconnect is performed by a process selected from the group including reflow bonding, thermal compression bonding or ultrasonic bonding.